

WE CLAIM:

1. One of a number of nodes of a communication system, the nodes being connected to a communication medium for transmitting data among the nodes, said one node comprising:
 - a communication controller, across which the node is connected to the communication medium, said communication controller having a synchronized clock signal;
 - a bus guardian for controlling access of said communication controller to the communication medium, said bus guardian having an electronic circuit generating a bus guardian internal clock signal which is less accurate than said synchronized clock signal, said bus guardian also having means for examining said synchronized clock signal using said internal clock signal; and
 - means for passing said synchronized clock signal to said examining means.
2. The node of claim 1, wherein said communication controller has an additional clock signal and further comprising means for passing said additional clock signal to said bus guardian, wherein said examining means has means for monitoring said synchronized clock signal using said additional clock signal and means for monitoring said additional clock signal using said bus guardian internal clock signal.
3. The node of claim 2, wherein said means for monitoring said additional clock signal count a number of internal clock signal periods during a configurable number of additional clock signal periods and determine whether a number of counted internal clock signal periods is within a configurable tolerance window.
4. The node of claim 2, wherein said means for monitoring said synchronized clock signal using said additional clock signal count a number of additional clock signal periods during a configurable number of synchronized clock signal periods and determine whether a number of counted additional clock signal periods is within a configurable tolerance window.
5. The node of claim 2, wherein said means for monitoring said additional clock signal using said internal clock signal count a number of internal clock signal periods during multiple additional clock signal periods.
6. The node of claim 2, wherein said means for monitoring said synchronized clock signal using said additional clock signal count a number of additional clock signal periods during multiple synchronized clock signal periods.
7. The node of claim 2, wherein at least one of said means for monitoring said additional clock signal and said means for monitoring said synchronized clock signal comprise a watchdog.
8. The node of claim 1, wherein said bus guardian internal clock signal is generated by means

of a resonant circuit comprising a resistance and a capacitance.

9. A method for monitoring a synchronized clock signal from a communication controller across which one of a number of nodes of a communication system is connected to a communication medium for transmitting data among the nodes, said node having a bus guardian for controlling access of the communication controller to the communication medium, the bus guardian having an electronic circuit generating a bus guardian internal clock signal which is less accurate than the synchronized clock signal, the method comprising the steps of:
 - a) passing the communication controller synchronized clock signal to the bus guardian; and
 - b) monitoring said synchronized clock signal using said internal clock signal.
10. The method of claim 9, further comprising providing an additional clock signal from the communication controller to the bus guardian, wherein the synchronized clock signal is monitored using the additional clock signal and the additional clock signal is monitored using the bus guardian internal clock signal.
11. The method of claim 10, wherein the additional clock signal is monitored by counting a number of internal clock signal periods during a configurable number of additional clock signal periods and determining whether a number of counted internal clock signal periods is within a configurable tolerance window.
12. The method of claim 10, wherein the synchronized clock signal is monitored by counting a number of additional clock signal periods during a configurable number of synchronized clock signal periods and determining whether a number of counted additional clock signal periods is within a configurable tolerance window.
13. A computer program, which is able to run on a computer or a microprocessor, wherein the computer program is programmed to execute the method of claim 9.
14. The computer program of claim 13, wherein the computer program is stored on one of a read-only-memory (ROM), a random-access-memory (RAM), and a flash-memory.
15. A computer programmed to execute the method of claim 9.
16. A data storage medium containing machine readable instructions for carrying of the method of claim 9.